Blakely, Sokoloff, Taylor & Zafman LLP (408) 947-8200 Title: Render-Cache Controller for Multithreading, Multi-Core Graphics

1st Named Inventor: Thomas A. Piazza Express Mail No.: EV 439337965 US

Sheet: 1 of 4

Docket No.: 42P19136

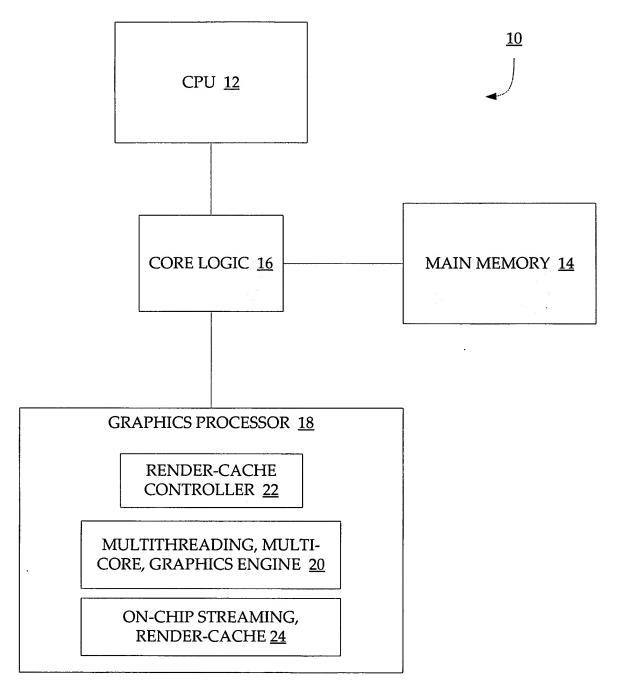


FIG. 1

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Graphics Processor

1st Named Inventor: Thomas A. Piazza Express Mail No.: EV 439337965 US Sheet: 2 of 4

Docket No.: 42P19136

CACHE 24 RENDER-(COLOR/Z) ACCESS PIXEL DATA 36 **®°** ₩ (B),(A) MULTITHREADING, MULTI-CORE MULTITHREADING, MULTI-CORE GRAPHICS PROCESSOR 18 **CORE5 CORE2** 38 \mathbf{I} T0T1 \mathbf{II} GRAPHICS ENGINE 20 PIPELINE(IN FLIGHT RESET FOR FIRST B and THEN A) CORE4 **CORE1** T010 Π Π **CORE0 CORE3** \mathbf{I} T0 Π \mathbf{II} (A), (B) DISPATCHER THREAD 34 CACHE-LINE (A,B) CONTROLLER **ALLOCATION** (GENERATES IN-FLIGHT CHECK 32 RENDER-CACHE RASTER PRE-2X2) 22 30 (a,b)

.†

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Graphics Processor

1st Named Inventor: Thomas A. Piazza Express Mail No.: EV 439337965 US

Sheet: 3 of 4

Docket No.: 42P19136

RENDER-CACHE CONTROLLER 22

CACHE-LINE STATUS ARRAY <u>40</u>

PIXEL MASK ARRAY <u>42</u>

TAG CONTENT ADDRESSABLE MEMORY (CAM) <u>44</u>

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Express Mail No.: EV 439337965 US Docket No.: 42P19136

Sheet: 4 of 4

